

AMENDMENTS TO THE CLAIMS

- 1 1. (Original) A transceiver circuit capable of transferring
2 data at one or more transfer rates, the transceiver circuit
3 comprising:
4 one or more state machines having one or more tone phases
5 in which determination of the maximum transfer rate for one
6 or more channels and one or more connections with one or
7 more remote devices is carried out through exchange of one
8 or more tone signals with at least one of the remote device
9 or devices, and one or more data transfer phases in which
10 data transfer is carried out at one or more frequencies
11 higher than that of at least one of the tone signal or
12 signals;
13 one or more error detection circuits detecting one or
14 more errors in one or more receive signals; and
15 one or more data transfer phase transition suppressor
16 circuits;
17 wherein, in the event that at least one of the error
18 detection circuit or circuits detects at least one of the
19 error or errors within at least one of the receive signal
20 or signals during at least one of the data transfer phase
21 or phases, one or more transitions is made from at least
22 one of the data transfer phase or phases to at least one of
23 the tone phase or phases, and after at least one of such
24 transition or transitions has occurred, at least one of the
25 data transfer phase transition suppressor circuit or
26 circuits carries out control so as to prevent transition
27 back to at least one of the data transfer phase or phases.
- 1 2. (Original) A transceiver circuit according to claim 1
2 further comprising:

3 one or more timers; and
4 one or more error counters;
5 wherein, only in the event that one or more numbers of
6 errors occurring within one or more fixed times as detected
7 by at least one of the error detection circuit or circuits,
8 at least one of the timer or timers, and at least one of
9 the error counter or counters during at least one of the
10 data transfer phase or phases is greater than at least one
11 preestablished value, one or more transitions is made from
12 at least one of the data transfer phase or phases to at
13 least one of the tone phase or phases, and after at least
14 one of such transition or transitions has occurred, at
15 least one of the data transfer phase transition suppressor
16 circuit or circuits carries out control so as to prevent
17 transition back to at least one of the data transfer phase
18 or phases.

1 3. (Original) A transceiver circuit according to claim 1
2 further comprising:
3 one or more transfer rate comparison circuits comparing
4 the minimum transfer rate of which the transceiver circuit
5 is capable and one or more transfer rates employed during
6 at least one of the data transfer phase or phases;
7 wherein, only in the event that at least one of the error
8 detection circuit or circuits detects at least one of the
9 error or errors and at least one of the transition or
10 transitions is made from at least one of the data transfer
11 phase or phases to at least one of the tone phase or phases
12 when at least one result of at least one comparison made by
13 at least one of the transfer rate comparison circuit or
14 circuits is that at least one of the transfer rate or rates
15 employed during at least one of the data transfer phase or
16 phases is identical to the minimum transfer rate or rates

17 of which the transceiver circuit is capable, at least one
18 of the data transfer phase transition suppressor circuit or
19 circuits carries out control so as to prevent transition
20 back to at least one of the data transfer phase or phases.

1 4. (Original) A transceiver circuit capable of transferring
2 data at one or more transfer rates, the transceiver circuit
3 comprising:

4 one or more state machines having one or more tone phases
5 in which one or more connections with one or more remote
6 devices are established through exchange of one or more
7 tone signals with at least one of the remote device or
8 devices, one or more speed negotiation phases in which
9 determination of the maximum transfer rate permitted by one
10 or more channels is carried out through mutual notification
11 of one or more transfer rates of which the local device is
12 capable, this notification being actually carried out at at
13 least one of such transfer rate or rates, and one or more
14 data transfer phases in which data transfer is carried out
15 at at least one of the transfer rate or rates determined at
16 at least one of the speed negotiation phase or phases;

17 one or more error detection circuits detecting one or
18 more errors in one or more receive signals; and

19 one or more speed negotiation phase transition suppressor
20 circuits;

21 wherein, in the event that at least one of the error
22 detection circuit or circuits detects at least one of the
23 error or errors within at least one of the receive signal
24 or signals during at least one of the data transfer phase
25 or phases, one or more transitions is made from at least
26 one of the data transfer phase or phases to at least one of
27 the tone phase or phases, and after at least one of such
28 transition or transitions has occurred, at least one of the

29 speed negotiation phase transition suppressor circuit or
30 circuits carries out control so as to prevent transition to
31 at least one of the speed negotiation phase or phases.

1 5. (Original) A transceiver circuit capable of transferring
2 data at one or more transfer rates, the transceiver circuit
3 comprising:

4 one or more state machines having one or more tone phases
5 in which one or more connections with one or more remote
6 devices are established through exchange of one or more
7 tone signals with at least one of the remote device or
8 devices, one or more speed negotiation phases in which
9 determination of one or more maximum transfer rates
10 permitted by one or more channels is carried out through
11 mutual notification of one or more transfer rates of which
12 the local device is capable, this notification being
13 actually carried out at at least one of such transfer rate
14 or rates, and one or more data transfer phases in which
15 data transfer is carried out at at least one of the
16 transfer rate or rates determined at at least one of the
17 speed negotiation phase or phases;

18 one or more error detection circuits detecting one or
19 more errors in one or more receive signals; and

20 one or more speed negotiation phase transition suppressor
21 circuits;

22 wherein, in the event that at least one of the error
23 detection circuit or circuits detects at least one of the
24 error or errors within at least one of the receive signal
25 or signals during at least one of the speed negotiation
26 phase or phases, one or more transitions is made from at
27 least one of the data transfer phase or phases to at least
28 one of the tone phase or phases, and after at least one of
29 such transition or transitions has occurred, at least one

30 of the speed negotiation phase transition suppressor
31 circuit or circuits carries out control so as to prevent
32 transition to at least one of the speed negotiation phase
33 or phases.

1 6. (Currently Amended) A transceiver circuit according to
2 claim 4 ~~or~~ 5 further comprising:
3 one or more timers; and
4 one or more error counters;
5 wherein, only in the event that one or more numbers of
6 errors occurring within one or more fixed times as detected
7 by at least one of the error detection circuit or circuits,
8 at least one of the timer or timers, and at least one of
9 the error counter or counters is greater than at least one
10 preestablished value, one or more transitions is made from
11 at least one of the data transfer phase or phases to at
12 least one of the tone phase or phases, and after at least
13 one of such transition or transitions has occurred, at
14 least one of the state machine phase transition suppressor
15 circuit or circuits carries out control so as to prevent
16 transition to at least one of the speed negotiation phase
17 or phases.

1 7. (Currently Amended) A transceiver circuit according to
2 claim 4 ~~or~~ 5 further comprising:
3 one or more transfer rate comparison circuits comparing
4 minimum transfer rate of which the transceiver circuit is
5 capable and one or more transfer rates employed during at
6 least one of the data transfer phase or phases;
7 wherein, only in the event that at least one of the error
8 detection circuit or circuits detects at least one of the
9 error or errors and at least one of the transition or
10 transitions is made from at least one of the data transfer
11 phase or phases to at least one of the tone phase or phases

when at least one result of at least one comparison made by at least one of the transfer rate comparison circuit or circuits is that at least one of the transfer rate or rates employed during at least one of the data transfer phase or phases is identical to at least one of the minimum transfer rate or rates of which the transceiver circuit is capable, at least one of the speed negotiation phase transition suppressor circuit or circuits carries out control so as to prevent transition to at least one of the speed negotiation phase or phases.

8. (Currently Amended) A transceiver circuit according to claim 4 ~~or 5~~ further comprising:

one or more counters; and

one or more timers;

wherein the transceiver circuit is OP i.LINK-compliant;

wherein at least one of the counter or counters counts one or more numbers of transitions from at least one of the tone phase or phases to at least one of the speed negotiation phase or phases; and

wherein, in the event that at least one of the number or numbers of transitions as counted by at least one of the counter or counters reaches at least one preestablished value within at least one fixed time, it being determined that channel quality is poor, at least one of the speed negotiation phase transition suppressor circuit or circuits carries out control so as to prevent transition to at least one of the speed negotiation phase or phases.

9. (Currently Amended) A transceiver circuit according to claim 2, ~~3, 6, 7, or 8~~ wherein:

one or more tone signal transmit select circuits are employed as at least one of the data transfer phase transition suppressor circuit or circuits or speed

6 negotiation phase transition suppressor circuit or
7 circuits; and

8 in the event that at least one of the error detection
9 circuit or circuits determines that channel quality is poor
10 and one or more transitions is made from at least one of
11 the data transfer phase or phases to at least one of the
12 speed negotiation phase or phases, at least one of the tone
13 signal transmit select circuit or circuits carries out
14 control so as to prevent transmission of one or more tone
15 signals.

1 10. (Original) A transceiver circuit according to claim 9
2 further comprising:

3 one or more receive signal detection circuits; and
4 one or more timers;

5 wherein, in the event that at least one of the receive
6 signal detection circuit or circuits and at least one of
7 the timer or timers establish during at least one of the
8 tone phase or phases that at least one receive signal,
9 being absent for not less than at least one fixed time, has
10 been completely disconnected, at least one of the tone
11 signal transmit select circuit or circuits reinitiates
12 transmission of one or more tone signals.

1 11. (Original) A transceiver circuit according to claim 9
2 further comprising:

3 one or more cable connect detection circuits;

4 wherein, in the event that at least one of the cable
5 connect detection circuit or circuits establishes during at
6 least one of the tone phase or phases that one or more
7 cables has been disconnected, at least one of the tone
8 signal transmit select circuit or circuits reinitiates
9 transmission of one or more tone signals after at least one
10 of the cable or cables has been reconnected.

1 12. (Currently Amended) A transceiver circuit according to
2 claim ~~2, 3, 6, 7, or 8~~ wherein:
3 one or more transmitter power supply control circuits are
4 employed as at least one of the data transfer phase
5 transition suppressor circuit or circuits or speed
6 negotiation phase transition suppressor circuit or
7 circuits; and
8 in the event that at least one of the error detection
9 circuit or circuits determines that channel quality is
10 poor, one or more transitions is made to at least one of
11 the tone phase or phases, and after at least one of such
12 transition or transitions has occurred, at least one of the
13 transmitter power supply control circuit or circuits causes
14 at least one power supply of at least one transmitter to be
15 turned OFF.

1 13. (Original) A transceiver circuit according to claim 12
2 further comprising:
3 one or more receive signal detection circuits; and
4 one or more timers;
5 wherein, in the event that at least one of the receive
6 signal detection circuit or circuits and at least one of
7 the timer or timers establish during at least one of the
8 tone phase or phases that at least one receive signal,
9 being absent for not less than at least one fixed time, has
10 been completely disconnected, at least one of the
11 transmitter power supply control circuit or circuits causes
12 at least one power supply of at least one transmitter to be
13 turned ON.

1 14. (Original) A transceiver circuit according to claim 12
2 further comprising:
3 one or more cable connect detection circuits;
4 wherein, in the event that at least one of the cable

5 connect detection circuit or circuits establishes during at
6 least one of the tone phase or phases that one or more
7 cables has been disconnected, at least one of the
8 transmitter power supply control circuit or circuits causes
9 at least one power supply of at least one transmitter to be
10 turned ON after at least one of the cable or cables has
11 been reconnected.

1 15. (Currently Amended) A transceiver circuit according to
2 claim 6, ~~7, or 8~~ wherein:

3 the transceiver circuit is OP i.LINK-compliant;
4 one or more TPBIAS mask circuits provided at one or more
5 PORT locations is or are employed as at least one of the
6 speed negotiation phase transition suppressor circuit or
7 circuits; and

8 in the event that at least one of the error detection
9 circuit or circuits determines that channel quality is
10 poor, one or more transitions is made to at least one of
11 the tone phase or phases, and thereafter at least one of
12 the TPBIAS mask circuit or circuits masks one or more
13 TPBIAS signals from at least one PHY carries out control so
14 as to prevent transmission of one or more long tones and/or
15 one or more continuous signals even if at least one TPBIAS
16 is active.

1 16. (Original) A transceiver circuit according to claim 15
2 further comprising:

3 one or more receive signal detection circuits; and
4 one or more timers;

5 wherein, in the event that at least one of the receive
6 signal detection circuit or circuits and at least one of
7 the timer or timers establish during at least one of the
8 tone phase or phases that at least one receive signal,
9 being absent for not less than at least one fixed time

10 following transmission of one or more tone signals by one
11 or more local transmit circuits, has been completely
12 disconnected, at least one of the mask or masks applied to
13 at least one of the TPBIAS signal or signals by at least
14 one of the TPBIAS mask circuit or circuits is removed,
15 causing one or more long tone signals and/or one or more
16 continuous signals to be transmitted when at least one
17 TPBIAS is active.

1 17. (Original) A transceiver circuit according to claim 15
2 further comprising:
3 one or more cable connect detection circuits;
4 wherein, in the event that at least one of the cable
5 connect detection circuit or circuits establishes during at
6 least one of the tone phase or phases that one or more
7 cables has been disconnected, at least one of the mask or
8 masks applied to at least one of the TPBIAS signal or
9 signals by at least one of the TPBIAS mask circuit or
10 circuits is removed after at least one of the cable or
11 cables has been reconnected, causing one or more long tone
12 signals and/or one or more continuous signals to be
13 transmitted when at least one TPBIAS is active.

1 18. (Currently Amended) A transceiver circuit according to
2 claim 6, ~~7, or 8~~ wherein:
3 the transceiver circuit is OP i.LINK-compliant;
4 one or more TPBIAS suppressor circuits provided at one or
5 more PHY locations is or are employed as at least one of
6 the speed negotiation phase transition suppressor circuit
7 or circuits; and
8 in the event that at least one of the error detection
9 circuit or circuits determines that channel quality is
10 poor, one or more transitions is made to at least one of
11 the tone phase or phases, and thereafter, even if at least

12 one TPBIAS is active within at least one of the PHY
13 location or locations, at least one of the TPBIAS
14 suppressor circuit or circuits carries out control so as to
15 prevent at least one of the PORT location or locations from
16 being notified of the fact that the at least one TPBIAS is
17 active.

1 19. (Original) A transceiver circuit according to claim 18
2 further comprising:
3 one or more receive signal detection circuits; and
4 one or more timers;
5 wherein, in the event that at least one of the receive
6 signal detection circuit or circuits and at least one of
7 the timer or timers establish during at least one of the
8 tone phase or phases that at least one receive signal,
9 being absent for not less than at least one fixed time
10 following transmission of one or more tone signals by one
11 or more local transmit circuits, has been completely
12 disconnected, at least one of the TPBIAS suppressor circuit
13 or circuits causes at least one of the PORT location or
14 locations to be notified of at least one value of at least
15 one TPBIAS signal within at least one of the PHY location
16 or locations.

1 20. (Original) A transceiver circuit according to claim 18
2 further comprising:
3 one or more cable connect detection circuits;
4 wherein, in the event that at least one of the cable
5 connect detection circuit or circuits establishes during at
6 least one of the tone phase or phases that one or more
7 cables has been disconnected, at least one of the TPBIAS
8 suppressor circuit or circuits, after at least one of the
9 cable or cables has been reconnected, causes at least one
10 of the PORT location or locations to be notified of at

11 least one value of at least one TPBIAS signal within at
12 least one of the PHY location or locations.

1 21. (Original) A transceiver circuit according to claim 6-
2 ~~7, or 8~~ wherein:

3 the transceiver circuit is OP i.LINK-compliant;
4 one or more BIAS_DETECT suppressor circuits provided at
5 one or more PORT locations is or are employed as at least
6 one of the speed negotiation phase transition suppressor
7 circuit or circuits; and

8 in the event that at least one of the error detection
9 circuit or circuits determines that channel quality is
10 poor, one or more transitions is made to at least one of
11 the tone phase or phases, and thereafter, even if one or
12 more long tones and/or one or more continuous signals is or
13 are received from one or more remote devices by at least
14 one of the PORT location or locations and at least one
15 BIAS_DETECT is active, at least one of the BIAS_DETECT
16 suppressor circuit or circuits carries out control so as to
17 prevent at least one of one PHY location or locations from
18 being notified of the fact that the at least one
19 BIAS_DETECT is active.

1 22. (Original) A transceiver circuit according to claim 21
2 further comprising:

3 one or more receive signal detection circuits; and
4 one or more timers;

5 wherein, in the event that at least one of the receive
6 signal detection circuit or circuits and at least one of
7 the timer or timers establish during at least one of the
8 tone phase or phases that at least one receive signal,
9 being absent for not less than at least one fixed time
10 following transmission of one or more tone signals by one
11 or more local transmit circuits, has been completely

12 disconnected, at least one of the BIAS_DETECT suppressor
13 circuit or circuits causes at least one of the PHY location
14 or locations to be notified of at least one value of at
15 least one BIAS_DETECT signal within at least one of the
16 PORT location or locations.

1 23. (Original) A transceiver circuit according to claim 21
2 further comprising:
3 one or more cable connect detection circuits;
4 wherein, in the event that at least one of the cable
5 connect detection circuit or circuits establishes during at
6 least one of the tone phase or phases that one or more
7 cables has been disconnected, at least one of the
8 BIAS_DETECT suppressor circuit or circuits, after at least
9 one of the cable or cables has been reconnected, causes at
10 least one of the PHY location or locations to be notified
11 of at least one value of at least one BIAS_DETECT signal
12 within at least one of the PORT location or locations.

1 24. (Currently Amended) A transceiver circuit according to
2 claim ~~6, 7, or 8~~ wherein:
3 the transceiver circuit is OP i.LINK-compliant;
4 one or more BIAS_DETECT mask circuits provided at one or
5 more PHY locations is or are employed as at least one of
6 the speed negotiation phase transition suppressor circuit
7 or circuits; and
8 in the event that at least one of the error detection
9 circuit or circuits determines that channel quality is
10 poor, one or more transitions is made to at least one of
11 the tone phase or phases, and thereafter, even if one or
12 more BIAS_DETECT signals is active, masking by at least one
13 of the BIAS_DETECT mask circuit or circuits of at least one
14 BIAS_DETECT signal from at least one of the PORT location
15 or locations carries out control so as to prevent at least

16 one of the PHY location or locations from being notified of
17 the fact that the at least one BIAS_DETECT signal is
18 active.

1 25. (Original) A transceiver circuit according to claim 24
2 further comprising:

3 one or more receive signal detection circuits; and
4 one or more timers;

5 wherein, in the event that at least one of the receive
6 signal detection circuit or circuits and at least one of
7 the timer or timers establish during at least one of the
8 tone phase or phases that at least one receive signal,
9 being absent for not less than at least one fixed time
10 following transmission of one or more tone signals by one
11 or more local transmit circuits, has been completely
12 disconnected, at least one of the mask or masks applied to
13 at least one of the BIAS_DETECT signal or signals by at
14 least one of the BIAS_DETECT mask circuit or circuits is
15 removed, causing at least one of the PHY location or
16 locations to be notified of the fact that at least one
17 BIAS_DETECT is active when the at least one BIAS_DETECT is
18 active.

1 26. (Original) A transceiver circuit according to claim 24
2 further comprising:

3 one or more cable connect detection circuits;

4 wherein, in the event that at least one of the cable
5 connect detection circuit or circuits establishes during at
6 least one of the tone phase or phases that one or more
7 cables has been disconnected, at least one of the mask or
8 masks applied to at least one of the BIAS_DETECT signal or
9 signals by at least one of the BIAS_DETECT mask circuit or
10 circuits is removed after at least one of the cable or
11 cables has been reconnected, causing at least one of the

12 PHY location or locations to be notified of the fact that
13 the at least one BIAS_DETECT is active when the at least
14 one BIAS_DETECT is active.

1 27. (Currently Amended) A transceiver circuit according to
2 claim ~~2, 3, 6, 7, or 8~~ wherein:
3 the transceiver circuit is IEEE 1394-compliant;
4 one or more suspend/disable control circuits provided at
5 one or more PHY locations is or are employed as at least
6 one of the speed negotiation phase transition suppressor
7 circuit or circuits; and
8 in the event that at least one of the error detection
9 circuit or circuits determines that channel quality is
10 poor, at least one of the suspend/disable control circuit
11 or circuits, during at least one of the tone phase or
12 phases, causes at least one PORT at which at least one
13 error is or was detected to enter at least one suspended
14 state and/or at least one disabled state.

1 28. (Original) A transceiver circuit according to claim 27
2 further comprising:
3 one or more receive signal detection circuits; and
4 one or more timers;
5 wherein, in the event that at least one of the receive
6 signal detection circuit or circuits and at least one of
7 the timer or timers establish during at least one of the
8 tone phase or phases that at least one receive signal,
9 being absent for not less than at least one fixed time
10 following transmission of one or more tone signals by one
11 or more local transmit circuits, has been completely
12 disconnected, at least one of the suspend/disable control
13 circuit or circuits causes termination of at least one
14 suspended state and/or at least one disabled state.

1 29. (Original) A transceiver circuit according to claim 27
2 further comprising:
3 one or more cable connect detection circuits;
4 wherein, in the event that at least one of the cable
5 connect detection circuit or circuits establishes during at
6 least one of the tone phase or phases that one or more
7 cables has been disconnected, at least one of the
8 suspend/disable control circuit or circuits causes
9 termination of at least one suspended state and/or at least
10 one disabled state after at least one of the cable or
11 cables has been reconnected.

1 30. (Currently Amended) A transceiver circuit according to
2 claim ~~2, 3, 6, 7, or 8~~ wherein:
3 one or more wait states is or are present between at
4 least one of the data transfer phase or phases and at least
5 one of the tone phase or phases; and
6 in the event that at least one of the error detection
7 circuit or circuits determines that channel quality is
8 poor, one or more transitions is made from at least one of
9 the data transfer phase or phases to at least one of the
10 wait state or states, and only if it is established during
11 at least one of the wait state or states that at least one
12 remote device has been completely disconnected therefrom is
13 at least one transition made to at least one of the tone
14 phase or phases.

1 31. (Original) A transceiver circuit according to claim 30
2 further comprising:
3 one or more receive signal detection circuits; and
4 one or more timers;
5 wherein, in the event that at least one of the receive
6 signal detection circuit or circuits and at least one of
7 the timer or timers establish during at least one of the

8 tone phase or phases that at least one receive signal,
9 being absent for not less than at least one fixed time
10 following transmission of one or more tone signals by one
11 or more local transmit circuits, has been completely
12 disconnected, at least one transition is made from at least
13 one of the wait state or states back to at least one of the
14 tone phase or phases.

1 32. (Original) A transceiver circuit according to claim 30
2 further comprising:
3 one or more cable connect detection circuits;
4 wherein, in the event that at least one of the cable
5 connect detection circuit or circuits establishes during at
6 least one of the tone phase or phases that one or more
7 cables has been disconnected, at least one transition is
8 made from at least one of the wait state or states back to
9 at least one of the tone phase or phases after at least one
10 of the cable or cables has been connected.

1 33. (Original) A transceiver circuit capable of transferring
2 data at a plurality of transfer rates, the transceiver
3 circuit comprising:
4 one or more state machines having one or more tone phases
5 in which one or more connections with one or more remote
6 devices are established through exchange of one or more
7 tone signals with at least one of the remote device or
8 devices, one or more speed negotiation phases in which
9 determination of the maximum transfer rate permitted by one
10 or more channels is carried out through mutual notification
11 of one or more transfer rates of which one or more local
12 devices is capable, this notification being actually
13 carried out at at least one of such transfer rate or rates,
14 and one or more data transfer phases in which data transfer
15 is carried out at at least one of the transfer rate or

16 rates determined at at least one of the speed negotiation
17 phase or phases;
18 one or more error detection circuits detecting one or
19 more errors in one or more receive signals; and
20 one or more transfer rate comparison circuits comparing
21 the minimum transfer rate of the transceiver circuit and
22 one or more transfer rates employed during at least one of
23 the data transfer phase or phases;
24 wherein, in the event that at least one of the error
25 detection circuit or circuits detects at least one of the
26 error or errors within at least one of the receive signal
27 or signals during at least one of the data transfer phase
28 or phases when at least one result of at least one
29 comparison made by at least one of the transfer rate
30 comparison circuit or circuits is that at least one of the
31 transfer rate or rates employed during at least one of the
32 data transfer phase or phases is greater than the minimum
33 transfer rate or rates of the transceiver circuit, one or
34 more transitions is made from at least one of the data
35 transfer phase or phases to at least one of the tone phase
36 or phases, and thereafter, the maximum transfer rate of the
37 transceiver circuit during at least one of the speed
38 negotiation phase or phases is set so as to be at least one
39 rate that is lower than at least one transfer rate employed
40 during at least one of the data transfer phase or phases.

1 34. (Original) A transceiver circuit according to claim 33
2 further comprising:

3 one or more receive signal detection circuits; and
4 one or more timers;

5 wherein, in the event that at least one of the receive
6 signal detection circuit or circuits and at least one of
7 the timer or timers establish during at least one of the

8 tone phase or phases that at least one receive signal,
9 being absent for not less than at least one fixed time
10 following transmission of one or more tone signals by one
11 or more local transmit circuits, has been completely
12 disconnected, the maximum transfer rate of the transceiver
13 circuit during at least one of the speed negotiation phase
14 or phases is returned to its original maximum transfer
15 rate.

1 35. (Original) A transceiver circuit according to claim 33
2 further comprising:
3 one or more cable connect detection circuits;
4 wherein, in the event that at least one of the cable
5 connect detection circuit or circuits establishes during at
6 least one of the tone phase or phases that one or more
7 cables has been disconnected, the maximum transfer rate of
8 the transceiver circuit during at least one of the speed
9 negotiation phase or phases is returned to its original
10 maximum transfer rate after at least one of the cable or
11 cables has been reconnected.

1 36. (Currently Amended) A transceiver circuit according to
2 claim 10 ~~or 13~~ wherein the at least one fixed time is not
3 less than 132 ms.

1 37. (Currently Amended) A transceiver circuit according to
2 claim 16, ~~19, 22, 25, 28, 31, or 34~~ wherein the at least
3 one fixed time is not less than 64 ms and not more than 132
4 ms.

1 38. (Currently Amended) A transceiving method substantially
2 effects manifestation of one or more transceiver circuits
3 according to any one of claims 1 ~~through 37~~.

39. (Currently Amended) A transceiver apparatus comprising:
one or more transceiver circuits substantially according to
any one of claims 1 ~~through 37~~; and
one or more external display apparatuses;
wherein, in the event that at least one of the error
detection circuit or circuits determines that channel quality
is poor during at least one of the data transfer phase or
phases or speed negotiation phase or phases, and at least one
of the transceiver circuit or circuits is in one or more
suppressed states selected from among the group consisting of
suppression with respect to transition to at least one of the
data transfer phase or phases, suppression with respect to
transition to at least one of the speed negotiation phase or
phases, and suppression with respect to maximum transfer rate
during at least one of the speed negotiation phase or phases,
one or more users are notified of such fact by means of at
least one of the external display apparatus or apparatuses.